2.0 Performance Specification

Signals input to and output from the CLM are described and specified in this section. The signals are grouped together according to function.

2.1 The I²C Bus

The I²C bus is a serial control bus which is used to communicate with and control other modules in the projector. It consists of two signals, SDA and SCL, which appear on backplane connector P1. SDA is bi-directional and carries data bits to and from the CLM. SCL outputs clock pulses during data transfers (one bit is transferred for each clock pulse). Devices attached to the bus must have open-drain or open collector outputs (there are pull-up resistors to +5V on the CLM). All devices must be "slaves", since SCL is implemented on the CLM as an output. Devices must not pull SCL low in order to interrupt a data transfer, as the CPU cannot respond properly. Important I²C bus specifications are listed below.

PARAMETER	MIN	MAX	UNIT
SCL clock frequency		100	kHz
Low period of the clock	4.7		us
High period of the clock	4.0		us
Rise time		1	us
Fall time		300	ns
Logic LOW level		1.5	Volts
Logic HIGH level	3.0		Volts
Bus capacitance		400	pF

A data transfer cycle begins with a start condition and ends with a stop condition. A start condition is defined by a HIGH-to-LOW transition of SDA while SCL is HIGH. A stop condition is defined by a LOW-to-HIGH transition of SDA while SCL is HIGH. When data is not being transferred, both lines remain HIGH. Data is transferred in eight bit bytes. Each byte is followed by an acknowledge bit from the receiving device. Any number of bytes can be transmitted during a single data transfer cycle (ie. between start and stop conditions). Maximum transfer rate is 100 kbits/s. The actual transfer rate is software dependent. The timing of a data transfer is shown in the diagram below.